Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A differential circuit ~~comprising a single transistor current mirror, including a capacitor connected to the transistor by a switch, and two current sources connected to the current mirror by respective and independent switches, the switch of one of the current sources being operated together with the capacitor switch so as to charge the capacitor and the switch of the other current source being operated so that the circuit operates as a source-follower amplifier with a current source load.~~comprising:

a first transistor that has a first drain and a first source;

a capacitor that is connected to a first gate of the first transistor;

a first switch that controls an electrical connection between the first gate and the first drain;

a second transistor that has a second drain and a second source;

a third transistor that has a third drain and a third source;

a second switch that controls an electrical connection between the first transistor and the second transistor; and

a third switch that controls an electrical connection between the first transistor and the third transistor,

the differential circuit being configured such that a first period in which the first transistor is electrically connected to the second transistor through the second switch does not overlap a second period in which the first transistor is electrically connected to the third transistor through the third switch.

2. (Currently Amended) ~~A~~The differential circuit ~~as claimed in claim 1~~according to claim 1,

wherein the ~~said switches are each implemented as an n-channel transistor.~~differential circuit is configured such that a first current flows through the first transistor and the second transistor during the first period.

3. (Currently Amended) ~~A~~The differential circuit ~~as claimed in~~according to claim 1, wherein ~~one or more of the current sources is implemented as an independent transistor.~~the differential circuit is configured such that a second current flows through the first transistor and the third transistor during the second period.

4. (Currently Amended) ~~A~~The differential circuit ~~as claimed in~~according to claim 1, wherein the ~~current sources are implemented by a single transistor with the gate thereof connected via the two said current source switches to respective voltage inputs.~~differential circuit is configured such that each of the second transistor and the third transistor functions as a current source.

5. (Currently Amended) ~~A~~The differential circuit ~~as claimed in claim 4,~~according to claim 1, wherein ~~at least one additional switch is connected to the gate of the said current source single transistor, the additional switch being operated by a drive signal which is independent of and non-overlapping with drive signals applied to the said current source switches and which operably applies an independent voltage to the gate of the said current source single transistor.~~the differential circuit is configured such that the first gate is electrically connected to the first drain through the first switch during the first period.

6. (Currently Amended) ~~A~~The differential circuit ~~as claimed in~~according to claim 1, wherein the ~~output of the current mirror is connected to a MOS input amplifier.~~differential circuit is configured such that the first switch and the second switch are controlled by an identical signal.

7. (Currently Amended) ~~A~~The differential circuit ~~as claimed in~~according to claim 1,

~~wherein the output of the current mirror is connected to the input of a second single transistor current mirror.~~further comprising an amplifier that is connected to the first transistor.

8. (Currently Amended) ~~A~~The differential circuit ~~as claimed in~~according to claim 1,

wherein the ~~said two current source switches are connected to the single transistor current mirror via a transistor pair comprising two transistors connected in parallel with each other and having their gates each effectively connected with a respective one of the said two current source switches, so as to receive the respective drive signal applied to the said two current source switches.~~differential circuit is configured such that any one of the second drain and the second source and any one of the third drain and the third source are electrically connected to a predetermined potential.

9. (Currently Amended) ~~A~~The differential circuit ~~as claimed in claim 8,~~according to claim 2,

wherein the ~~output of the said single transistor current mirror is connected to a self bias comparator via the said transistor pair.~~differential circuit is configured such that a charge corresponding to the first current is charged to the capacitor during the first period.

10. (Currently Amended) ~~A~~The differential circuit ~~as claimed in claim 1,~~according to claim 9,

wherein ~~current source connectable so that the circuit operates as a source follower amplifier with a current source load is the output of a sensor pixel of an active matrix sensor array.~~the differential circuit is configured such that the first gate is electrically connected to the first drain through the first switch.

11. (Currently Amended) ~~An electronic device having a~~The differential circuit ~~as claimed in claim 1.~~according to claim 1,

wherein the differential circuit is configured such that the differential circuit amplifies an output of a sensor pixel.

12. (New) An electronic device comprising the differential circuit according to claim 1.